CLAIMS

1. An integrated MOS VGA having improved dynamic range comprising:

a substrate;

a first differential pair amplifier disposed upon the substrate and coupled to a VGA output having a gain contributing to VGA gain in direct proportion to the first differential pair amplifier gain;

a second differential pair amplifier disposed upon the substrate and coupled to the VGA output having a gain, and coupled to the first differential amplifier such that an increase in second differential pair amplifier gain contributes in inverse proportion to the VGA gain; and

a fixed control current split between the first differential pair amplifier and the second differential pair amplifier such that current to the second differential pair amplifier source connection is not greater than current applied to the first differential pair amplifier source connection and applied such that an increase in current causes an increase in amplifier gain.

2. The integrated MOS VGA of claim 1 further comprising:

a variable voltage source coupled to the VGA output controlling differential pair gain; and

a control signal applied to the variable voltage source to control its level.

3. An integrated MOS VGA having an improved dynamic range comprising:

a differential variable gain amplifier; and

a linearization circuit producing a pair of currents simultaneously applied to the integrated MOS VGA, consisting of a first current and a second current that are applied to the

integrated MOS VGA for controlling amplifier gain, such that when the first current increases VGA gain tends to increase, and that when the second current increases VGA gain tends to decrease.

4. The integrated MOS VGA of claim 3 in which the linearization circuit further comprises the first current maintaining a value greater than the second current.

5. A method for providing, over a wide range of input signal voltages, variable gain amplification having a linear change in output current gain at a differential current output port as a function of a change in differential voltage input at a differential voltage input port, comprising the steps of:

providing an input control voltage derived from the differential input voltage;

providing a variable gain amplifier responsive to the differential input voltage, the variable gain amplifier having:

a first common source differential pair amplifier, the first common source differential pair amplifier having first common source differential pair output drains;

a second common source differential pair amplifier, the second common source differential pair amplifier having second common source differential pair output drains; and

the first common source differential pair output drains and the second common source differential pair output drains being connected in parallel to form the differential current output port and being responsive to the differential input voltage to provide the output current gain at the differential current output port;

deriving a first variable gain control signal from the input control voltage and providing the first variable control signal to the first common source differential pair amplifier to control maximizing gain of the first common source differential pair

amplifier when the input control voltage is low and minimizing gain of the first common source differential pair amplifier when the input control voltage is high;

deriving a second variable gain control signal from the input control voltage and providing the second variable gain control signal to the second common source differential pair amplifier to control minimizing gain of the second common source differential pair amplifier when the input control voltage is low and maximizing gain of the second common source differential pair amplifier when the input control voltage is high;

maintaining the first gain control signal in relationship to the second gain control signal such that the second gain control signal is less than the first gain control signal; and

reducing first common source differential pair amplifier drain-source Vds voltages and second common source differential pair amplifier drain-source Vds voltages as the differential input voltage increases.

6. The method of claim 5 wherein the step of reducing includes the step of reducing absolute direct current voltage at the differential current output port.

7. The method of claim 6 wherein the step of reducing absolute direct current voltage includes the steps of:

coupling a voltage control source across the differential current output port; and

inputting a third gain control signal derived from the input control voltage to control the voltage control source to reduce absolute direct current voltage at the differential current output port as the differential input voltage increases.

8. A method for providing, over a wide range of input signal voltages, variable gain amplification having a linear change in output signal current gain as a function of a change in differential input voltage, comprising the steps of:

providing the an input control voltage derived from the differential input voltage;

providing a variable gain amplifier responsive to the differential input voltage, the variable gain amplifier having:

a first transistor, the first transistor having a first transistor gate, a first transistor source and a first transistor drain, a first transistor drain-source Vds voltage being provided across the first transistor source and first transistor drain;

a second transistor, the second transistor having a second transistor gate, a second transistor source and a second transistor drain, a second transistor drain-source Vds voltage being provided across the second transistor source and second transistor drain;

a third transistor, the third transistor having a third transistor gate, a third transistor source and a third transistor drain, a third transistor drain-source Vds voltage being provided across the third transistor source and third transistor drain;

a fourth transistor, the fourth transistor having a fourth transistor gate, a fourth transistor source and a fourth transistor drain, a fourth transistor drain-source Vds voltage being provided across the fourth transistor source and fourth transistor drain;

the first transistor gate and the fourth transistor gate being responsive to a first input voltage level of the input voltage differential, the second transistor gate and the third transistor gate being responsive to a second input voltage level, the first transistor source being coupled to the second transistor source, the third transistor source being coupled to the fourth transistor source, the second transistor drain being

coupled to the fourth transistor drain to provide a first output current level of the output current differential, the first transistor drain being coupled to the third transistor drain to provide a second output current level of the output current differential;

deriving a first variable gain control signal from the control signal and providing the first variable gain control signal to the first transistor source and to the second transistor source such that both the gain of the first transistor and the gain of the second transistor can be maximized when the input control voltage is low and can be minimized when the input control voltage is high;

deriving a second variable gain control signal from the control signal and providing the second variable gain control signal to the third transistor source and to the fourth transistor source such that both a third transistor gain and a fourth transistor gain can be minimized when the input control voltage is low and can be maximized when the input control voltage is high;

maintaining the first gain control signal in relationship to the second gain control signal such that the second gain control signal is less than the first gain control signal; and

reducing the first transistor Vds voltage, the second transistor Vds voltage, the third transistor Vds voltage and the fourth transistor Vds voltage as the differential input voltage increases.

9. The method of claim 8 wherein the step of reducing includes the step of reducing absolute direct current voltage at the first transistor drain, the second transistor drain, the third transistor drain and the fourth transistor drain.

10. The method of claim 9 wherein the step of reducing absolute direct current voltage includes the steps of:

providing a fifth transistor, the fifth transistor having a fifth transistor gate, a fifth transistor source and a fifth transistor drain, the fifth transistor source being coupled to the first transistor drain and to the third transistor drain;

providing a sixth transistor, the sixth transistor having a sixth transistor gate, a sixth transistor source and a sixth transistor drain, the sixth transistor source being coupled to the second transistor drain and to the fourth transistor drain;

providing a linear amplifier, the linear amplifier having a first linear amplifier output coupled to the fifth transistor gate, a second linear amplifier output coupled to the sixth transistor gate, a first linear amplifier input being coupled to the fifth transistor drain, a second linear amplifier input being coupled to the sixth transistor drain; and

deriving a third gain control signal from the control signal to control the linear amplifier such that absolute direct current voltage at the first transistor drain, the second transistor drain, the third transistor drain and the fourth transistor drain is reduced as the differential input voltage increases.